

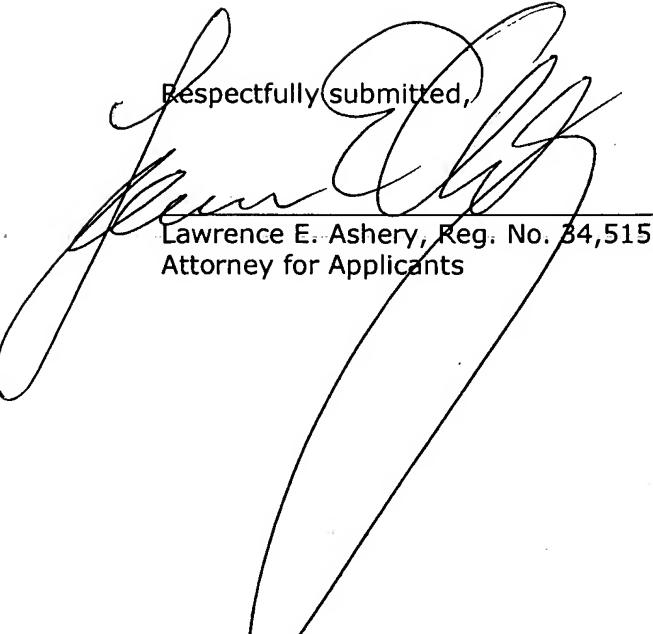
**Amendment to the Abstract:**

The Abstract has been amended. A revised Abstract is attached.

**ABSTRACT**

A power supply device has a capacitor unit (7) in which capacitors are interconnected in series, a charging unit (8) for charging the capacitor unit (7) at a constant current, a detecting unit (6) for detecting voltage on the high potential side of each of the capacitors, a determining unit (4) for determining the existence of an abnormality based on the voltage detected by the detecting unit (6). The determining unit determines the abnormality when the difference between respective voltages on the high potential sides of some adjacent capacitors exceeds upper-limit voltage value Va, when the difference is lower than lower-limit voltage value Vb, or when a voltage is negative.

Respectfully submitted,

  
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Attachments: Abstract

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DENNIS McDERMOTT

DESCRIPTION PCT/PTO 17 JUL 2006

POWER SUPPLY DEVICE

THIS APPLICATION IS A U.S. NATIONAL PHASE APPLICATION OF  
PCT INTERNATIONAL APPLICATION PCT/JP2005/022836.

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TECHNICAL FIELD

The present invention relates to detection of an abnormality of a capacitor in a power supply device for storing electricity in the capacitor.

10 BACKGROUND ART

A capacitor unit of a large capacity used for storing electricity of the power supply device is generally used for stabilizing a main power supply during load variation. The severest application is usage as a power supply for a backup operation when the main power supply fails. High reliability is 15 required when the capacitor unit is applied to a braking system mounted in a vehicle, for example. For detecting a degradation state of the capacitor unit, a method is known, in which resistance or capacity of the capacitor unit is measured and the degradation state of the capacitor unit during charge is monitored. Additionally, another method is known in which a discharge 20 circuit disposed in parallel with a capacitor disposed in the capacitor unit is operated and the voltage of the capacitor is brought into balance when a predetermined voltage or higher is applied to the capacitor.

As conventional art document information related to the present invention, Japanese Patent Unexamined Publication No. H10-174285 is known, 25 for example.

However, even when an abnormality occurs in a single capacitor, it is disadvantageously difficult to detect the abnormality as a large variation in the whole capacitor unit. When a balance operation circuit fails, the abnormality

cannot be detected. When a backup operation by the capacitor unit is required in an emergency state, the operation is not guaranteed.

## SUMMARY OF THE INVENTION

5 A power supply device of the present invention has the following elements: a capacitor unit in which capacitors are interconnected in series or in series-parallel; a charging unit for charging the capacitor unit at a constant current; a detecting unit for detecting voltage on the high potential side of each of the capacitors; a determining unit for determining the existence of an 10 abnormality based on the voltage detected by the detecting unit; and a communication unit for outputting a determining result from the determining unit. The determining unit determines the abnormality when difference between respective voltages on the high potential sides of some adjacent capacitors exceeds upper-limit voltage value  $V_a$ , when the difference is lower 15 than lower-limit voltage value  $V_b$ , or when one of respective voltages is negative. Thus, by detecting an abnormal voltage applied to each capacitor or a short failure, the abnormality detection of the capacitor unit is enabled, and hence the high reliability can be guaranteed.

## 20 BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 is a block diagram of a power supply device in accordance with an exemplary embodiment of the present invention.

Fig. 2 is a diagram explaining the voltage on the high potential side of the capacitor unit in accordance with the exemplary embodiment.

25 Fig. 3 is a diagram explaining the relation between the cell-short time and a case in which a cell is in short-circuiting and there is a capacity variation in the capacitor unit in accordance with the exemplary embodiment.

Fig. 4 is a diagram showing a case where the capacitor unit is formed by series-parallel connection, in which  $N$  capacitors are interconnected in series-parallel where  $M$  series are interconnected, in accordance with the exemplary embodiment.

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#### **REFERENCE MARKS IN THE DRAWINGS**

1	<u>battery</u>
2	<u>power supply device</u>
3	<u>electronic device mounted on a vehicle</u>
10	4 <u>determining unit</u>
	5 <u>communication unit</u>
	6 <u>detecting unit</u>
	7 <u>capacitor unit</u>
	8 <u>charging unit</u>
15	9 <u>communication output terminal</u>
	10 <u>backup output terminal</u>

#### **DETAILED DESCRIPTION OF PREFERRED EMBODIMENT**

##### **(EXEMPLARY EMBODIMENT)**

20 An exemplary embodiment of the present invention will be hereinafter described with reference to the drawings. Fig. 1 is a block diagram of a power supply device having capacitors for storage as an emergency backup power supply device for an electronic device mounted on a vehicle.

25 For extending the life of capacitor unit 7 formed of electrical double layer capacitors, capacitor unit 7 is needed to be kept in no charge state while being not used. The capacitor unit is discharged when a user gets off a vehicle, and is charged from a battery when the user gets on the vehicle. When the

capacitor unit is recharged as necessary in use, it is charged at a constant current by charging unit 8. When battery 1 comes off to turn off power, namely in an emergency, capacitor unit 7 applies energy to electronic device 3 mounted on the vehicle through backup output terminal 10.

5 Fig. 2 is a diagram explaining the voltage on the high potential side of the capacitor unit in accordance with the exemplary embodiment of the present invention. In capacitor unit 7 of Fig. 2, N capacitors 71, 72, 73 ... 7N are interconnected in series, and the both ends thereof are connected to output terminal 110 and ground terminal 120, respectively. The example where all of  
10 capacitors 71 through 7N are interconnected in series is described hereinafter, but they may be interconnected in series-parallel. The N is called series number. In other words, only series connection is employed as in Fig. 2, the number of capacitors is equivalent to series number N. Fig. 4 is a diagram showing a case where a capacitor unit of the exemplary embodiment of the  
15 present invention is formed by series-parallel connection, in which N capacitors are interconnected in series-parallel where M series are interconnected in parallel. Assuming N is 4 and M is 3, for example in Fig. 4, four capacitors are interconnected in series and three series of capacitors are interconnected in parallel, thereby forming a capacitor unit in a matrix shape. In this case,  
20 series number N is 4.

While capacitor unit 7 is being charged, detecting unit 6 monitors voltage during charge of each capacitor, and transmits the voltage value to determining unit 4. The voltage applied to a capacitor is determined as the difference between respective voltages on the high potential sides of the capacitor and its  
25 adjacent capacitor, as shown in Fig. 2. For example, the voltage value on the high potential side of the uppermost capacitor 71 is  $V_{h1}$  and the voltage value on the high potential side of capacitor 72 just described under capacitor 71 is

Vh2, so that the voltage applied to the uppermost capacitor 71 is determined as Vh1 – Vh2. Note that one side of the lowermost capacitor 7N is connected to ground terminal 120, so that the potential on this side is zero. The voltage applied to capacitor 7N is determined as VhN without taking difference.

5 It is recommended that upper-limit voltage value Va determined by determining unit 4 is set as withstand voltage value Vt per capacitor cell.

When there's no capacity variation among capacitors, the voltage of each capacitor is usually defined as 1/N of charge voltage Vc applied between output terminal 110 and ground terminal 120 of the capacitor unit. When an 10 abnormality occurs in the charge circuit or there are capacity variations of the capacitors, however, an abnormality such as disablement of charge and a short failure can be determined when the voltage of a capacitor is lower than at least half of the above-mentioned value, namely

$$Vc / (2N).$$

15 Therefore, lower-limit voltage value Vb determined by determining unit 4 is set at this value. When the voltage of a capacitor is negative, an abnormality is determined for securing safety of the circuit or the capacitor.

Next, voltage at which the determination is started is described.

Fig. 3 is a diagram showing the relation between the cell-short time 20 and explaining a case in which a cell is in short-circuiting and there is a capacity variation in the capacitor unit in accordance with the exemplary embodiment. When there is the capacity variation of the capacitors and a short failure occurs, the voltage corresponding to the short-failed capacitor is additionally applied to the remaining capacitors as shown in Fig. 3. Degree of the capacity variation 25 is shown by "dev". When the lowermost capacitor 70N has value  $C \times (1 - dev)$ , namely the lower limit of the capacity variation, and the remaining capacitors have value  $C \times (1 + dev)$ , namely the upper limit of the capacity variation, for

example as shown in Fig. 3, voltage  $V_k$  in charging the lowermost capacitor 70N is maximum.

Assuming that the number of series stages including a capacitor having short failure is at  $M$ , and the series number is at  $N$ . Also assuming that, one 5 capacitor of the capacitors that are not short-failed has the lower-limit capacity variation value, and the remaining capacitors have the upper-limit capacity variation value. At this time, when the voltage value in charging the capacitor having the lower-limit capacity variation value is set at  $V_k$ , and the voltage value in charging the capacitor having the upper-limit capacity variation value 10 is set at  $V_j$ , the following relation is satisfied,

$$V_k + (N - 1 - M) \times V_j = V_c \quad (\text{Eq. 1}).$$

Number  $M$  of series stages is the number of short-failed capacitors in the case of only series connection of Fig. 3. In the case of series-parallel connection, even if only one of the capacitors in the series direction is short-failed, the other 15 capacitor connected to the capacitor in parallel is in short-circuiting. Therefore, the number of stages (parallel direction) including the short-failed capacitors is set at  $M$ . As a result, when a plurality of capacitors in the same stage are short-failed,  $M$  is counted as one.

The same charge current flows through the capacitors interconnected in 20 series, so that the capacity of each capacitor is inversely proportional to the voltage at charge time. Therefore, the following relation is satisfied,

$$V_k / V_j = (1 + \text{dev}) / (1 - \text{dev}) \quad (\text{Eq. 2}).$$

Using the two equations,  $V_k$  is derived as below,

$$V_k = V_c \times \{ 1 / (1 - \text{dev}) \} / \{ (N - 1 - M) / (1 + \text{dev}) + 1 / (1 - \text{dev}) \} \quad (\text{Eq. 3}).$$

25 When voltage value  $V_k$  is set as withstand voltage value  $V_t$  of the capacitor, voltage value  $V_c$  at charge time at this time is derived using  $V_t$  as below,

$$V_c = V_t \times \{ 1 + (N - 1 - M) \times (1 - \text{dev}) / (1 + \text{dev}) \} \quad (\text{Eq. 4}).$$

Therefore, considering that  $V_c$  includes detection error margin  $\alpha$  such as a measuring error, predetermined voltage value  $V_d$  at the start of determination is set as below,

5  $V_d = V_t \times \{ 1 + (N - 1 - M) \times (1 - \text{dev}) / (1 + \text{dev}) \} - \alpha.$

Therefore, when the determination is started at the time when  $V_c$  is voltage value  $V_d$  or lower, the abnormality can be detected before over-voltage is applied to the capacitor at abnormal time. Specifically, when the full charge voltage of the capacitor is set at  $V_f$ , for example, it is recommended that the 10 determination is performed by the time when  $V_c$  reaches  $V_d = 0.8 V_f$ .

When these abnormalities are determined, communication unit 5 transmits a signal indicating the abnormalities from communication output terminal 9 to an external system such as an electronic device 3 mounted on a vehicle efshown in Fig. 31. Thus, the external system can secure a safe 15 operation as the whole system.

As a result, the abnormality of the capacitor can be detected, and high reliability can be achieved. Additionally, determination processing that handles many capacitors does not need to be started just after the start of the charge of capacitors. Here, at the start time of the charge, control processing 20 becomes dense and the load of the calculation processing becomes heavy. The determination processing may be started at the time when the load of the calculation processing is light at  $V_d$  or lower, for example at the time of  $V_c = 0.5 V_f$ . Therefore, the load of the calculation processing is light, such determination processing is useful in abnormality detection, and the advantage 25 is large.

## INDUSTRIAL APPLICABILITY

A power supply device of the present invention for determining an abnormality of a capacitor has high reliability, and is useful as a power supply device for charging the capacitor.